REMARKS

This application has been carefully reviewed in light of the Office Action dated December 14, 2004. Applicant has amended claims 1 and 8. Reconsideration and favorable action in this case are respectfully requested.

The Examiner has requested that the cross-reference to a prior US case be updated. Applicant has accordingly amended the first paragraph of page 1.

The Examiner has rejected claims 1-5, 7 under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 5,906,000 to Abe in view of U.S. Pat. No. 4,449,183 to Flahive. Applicant has reviewed these references in detail and does not believe that they disclose or make obvious the invention as claimed.

The Examiner has rejected claims 8, 9 and 11 under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 4,814,974 to Narayanan in view of U.S. Pat. No. 5,581,722 to Welland. Applicant has reviewed these references in detail and does not believe that they disclose or make obvious the invention as claimed.

The Examiner has rejected claim 12 under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 4,814,974 to Narayanan in view of U.S. Pat. No. 5,581,722 to Welland and further in view of U.S. Pat. No. 5,918,160 to Lysejko. Applicant has reviewed these references in detail and does not believe that they disclose or make obvious the invention as claimed.

Applicant notes with appreciation that the Examiner has indicated that claim 6 would be allowable if rewritten in independent form.

Applicant believes that the claims are directed to an invention that is much different than that shown in the cited references. The Abe reference is directed to a cache controller for use with a single CPU. Each entry in the cache memory 18 contains a tag

area and a data area. The tag area (Figure 2) includes a valid/invalid flag 40 for the entry, a priority 42 for the data in the data area and an address indicative of the original location of the data (col. 4, lines 16-21). The priority for an entry is indicative of the frequency of access by the CPU 10 for accessing the data stored in the entry (col. 3, lines 61-64).

A cache memory stores a small subset of a main memory in a high speed memory to allow faster access to data from the main memory that has already been read. As more memory locations are read, some entries in the cache memory will be replaced with data from a different main memory location. The "priority" in the cache memory 18 of Abe is used to determine whether data from a currently read memory location in main memory *will replace the presently stored entry in the cache* (column 5, lines 38-51). The priority described in Abe has nothing whatsoever to do with access to a shared resource and specifically does not prioritize access based on an address space associated with an access request.

Even if combined with the Flahive reference, the combination would only show a multi-processor system where the replacement algorithm for a cache memory prioritized replacement of a cache entry. The combination would not show prioritization of access to the shared resource based at least in part on the address associated with the request.

The Narayanan reference shows a system for assigning priority between multiple devices (0-15) on a bus 28. Only a single device may transmit on the bus 28 at a time. An arbitrator 27 determines which device has priority (col. 4, lines 8-12). When a plurality of devices 0-15 request use of the bus 28 substantially simultaneously, or while the bus 28 is in use, the arbitrator 27 selects one of the requests according to some order of priority and signals the selected device 0-15 that it has been granted access (col. 4, lines 23-30).

The arbitrator 27 assigns sixteen levels of priority to the sixteen devices 0-15. The priority for each device is provided by a priority designator 24 (col. 4, lines 48-53).

Priority generators 71-86 specify the device associated with each priority level. In the embodiment described in column 7 of Narayanan, along with Figure 5, a memory 200 is used to hold different prioritization scenarios. Each word 202 has sixteen four bit fields. Each field associates a device 0-15 with a priority level (1-16). The priority of the devices is set by an address generator 201 which selects a word 202 from the memory 200 for output.

Narayanan is an example of device-based priority; i.e., pending access requests to a shared resource are prioritized according to the priority assigned to the particular devices that issued the requests. Welland and Flahive do not add subject matter that would change the prioritization scheme of Narayanan.

By contrast to the afore-mentioned references, in the present invention defined by claim 1, prioritizing access to a shared resource in a digital system having a plurality of devices vying for access to the shared resource is accomplished by organizing the address space of the shared resource into address space regions and *assigning individual access priority values to a plurality of the address space regions*. An access request specifies a target address within the address space of the shared resource and an access priority value is provided with the access request, *such that the access priority value corresponds to an access priority value assigned to an address space region selected by the target address*. Arbitration between multiple pending requests to the shared resource for access to the shared resource is based at least in part by using the access priority value assigned to each pending request.

The references cited by the examiner do not show the step of assigning priority values to address space regions, providing the priority value with an access request, or arbitrating between pending access request based on the priority values.

Similarly, in independent claim 8, a digital system comprises a shared resource and a plurality of devices connected to access the shared resource. A plurality of memory

management units (MMU) are connected to receive an address from a respective one of the plurality of devices, wherein each MMU has storage circuitry for storing a plurality of page entries and each page entry has an access priority field, each MMU being operable to output *an access priority value associated with a received address*. Arbitration circuitry is connected to receive a request signal from each of the plurality of devices and an associated access priority value from each MMU, *wherein the arbitration circuitry is operable to schedule access to the shared resource according to the access priority values*.

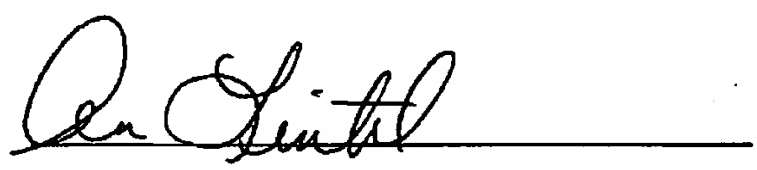
Once again, the references cited by the Examiner do not show prioritization based on priority values associated with a page entry.

The Commissioner is hereby authorized to charge any fees or credit any overpayment, including extension fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Alan W. Lintel, Applicant's Attorney at (972) 664-9595 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,



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